Pending Claims

The listing of claims will replace all prior versions, and listings of claims in the application.

Claim 1. (Cancelled).

Claim 2. (Previously Presented) A microprocessor for executing a set of instructions, comprising:

a register file including a first plurality of registers and a second plurality of registers;

a first functional unit that executes an integer operation in response to a first instruction, wherein said first instruction specifies a register to access within said first plurality of registers or said second plurality of registers, and wherein said first functional unit is adapted to access said first plurality of registers or said second plurality of registers as specified by said first instruction, to read an integer operand from either said first plurality of registers or said second plurality of registers as specified by said first instruction, and to write a result value to said first plurality of registers or said second plurality of registers as specified by said first instruction; and

a second functional unit that executes a floating point operation in response to a second instruction, wherein said second instruction specifies a register to access within said second plurality of registers, and wherein said second functional unit is adapted to access said second plurality of registers as specified by said second instruction, to read a

floating point operand from said second plurality of registers as specified by said second instruction, and to write a result value to said second plurality of registers as specified by said second instruction.

Claim 3. (Previously Presented) The microprocessor of claim 2, wherein said register file further includes a third plurality of registers, and wherein the microprocessor further comprises:

a third functional unit that performs a Boolean combinatorial operation in response to a third instruction, wherein said third instruction specifies a register to access within said third plurality of registers, and wherein said third functional unit is adapted to access said third plurality of registers as specified by said third instruction, to read a Boolean operand from said third plurality of registers as specified by said third instruction, and to write a result value to said third plurality of registers as specified by said third instruction.

Claim 4. (Previously Presented) The microprocessor of claim 2, wherein said integer operand is 32 bits wide.

Claim 5. (Previously Presented) The microprocessor of claim 2, wherein said floating point operand is 32 bits wide.

Claim 6. (Previously Presented) The microprocessor of claim 2, wherein said first functional unit and said second functional unit are configured to execute a plurality of instructions simultaneously.

Claim 7. (Previously Presented) A microprocessor for executing a set of instructions, comprising:

a plurality of register banks;

a first functional unit that executes an integer operation in response to a first instruction, wherein said first instruction specifies a register to access within a first plurality of registers or a second plurality of registers within one of said plurality of register banks, and wherein said first functional unit is adapted to access said first plurality of registers or said second plurality of registers as specified by said first instruction, to read an integer operand from either said first plurality of registers or said second plurality of registers as specified by said first instruction, and to write a result value to said first plurality of registers or said second plurality of registers as specified by said first instruction; and

a second functional unit that executes a floating point operation in response to a second instruction, wherein said second instruction specifies a register to access within said second plurality of registers, and wherein said second functional unit is adapted to access said second plurality of registers as specified by said second instruction, to read a floating point operand from said second plurality of registers as specified by said second instruction, and to write a result value to said second plurality of registers as specified by said second instruction.

Claim 8. (Previously Presented) The microprocessor of claim 7, further comprising:

a third functional unit that performs a Boolean combinatorial operation in response to a third instruction, wherein said third instruction specifies a register to access within a third plurality of registers within said one of said plurality of register banks, and wherein said third functional unit is adapted to access said third plurality of registers as specified by said third instruction, to read a Boolean operand from said third plurality of registers as specified by said third instruction, and to write a result value to said third plurality of registers as specified by said third instruction.

Claim 9. (Previously Presented) The microprocessor of claim 7, wherein said integer operand is 32 bits wide.

Claim 10. (Previously Presented) The microprocessor of claim 7, wherein said floating point operand is 32 bits wide.

Claim 11. (Previously Presented) The microprocessor of claim 7, wherein said first functional unit and said second functional unit are configured to execute a plurality of instructions simultaneously.

Claim 12. (Previously Presented) A microprocessor comprising:

a register file including a first plurality of registers and a second plurality of registers;

an instruction execution unit including:

an integer functional unit adapted to execute instructions having at least one source and one destination, each instruction indicating whether said at least one source and said at least one destination reside in said first plurality of registers or said second plurality of registers, and wherein said at least one source and said at least one destination each store an integer value; and

a floating point functional unit adapted to execute instructions having at least one source and at least one destination in said second plurality of registers, wherein said at least one source and said at least one destination each store a floating point value; and

a switching and multiplexing control unit connected between said integer functional unit and said register file, wherein said switching and multiplexing control unit is adapted to permit said integer functional unit to access said first plurality of registers or said second plurality of registers.

Claim 13. (Previously Presented) The microprocessor of claim 12, wherein said register file further includes a third plurality of registers, and

wherein said instruction execution unit further includes a Boolean functional unit adapted to execute Boolean combinatorial instructions having at least one source and at least one destination in said third plurality of registers, wherein said at least one source and said at least one destination each store a Boolean value.

Claim 14. (Previously Presented) The microprocessor of claim 12, wherein said floating point functional unit and said integer functional unit are configured to execute a plurality of instructions simultaneously.

Claim 15. (Previously Presented) The microprocessor of claim 12, wherein said integer value is 32 bits wide.

Claim 16. (Previously Presented) The microprocessor of claim 12, wherein said floating point value is 32 bits wide.